Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Currently amended) An electronic system comprising:

a first integrated circuit comprising:

an input buffer coupled between a first supply terminal and a second supply terminal and having an input directly connected to a pad; and

a clamp diode coupled between the pad and the first supply terminal; ~~and~~

a resistor having a first terminal coupled to the pad, and a second terminal coupled to receive an input signal; and

a second integrated circuit coupled to the second terminal of the resistor to provide the input signal,

wherein the resistor is not on the first integrated circuit or the second integrated circuit.

Claim 2. (Currently amended) The electronic system of claim 1 further comprising:

a switch coupled in series with the clamp diode ~~a second integrated circuit coupled to the second terminal of the resistor to provide the input signal~~.

Claim 3. (Previously presented) The electronic system of claim1 wherein the clamp diode has an anode and a cathode, the anode is coupled to the pad, and the cathode is coupled to the first supply terminal.

Claim 4. (Previously presented) The electronic system of claim 3 wherein the first supply terminal receives a positive supply voltage, and the second supply terminal receives a ground supply.

Claim 5. (Previously presented) The electronic system of claim 1 wherein the integrated circuit further comprises:

a pull-up output device coupled between the first supply terminal and the pad; and

a pull-down output device coupled between the pad and the second supply terminal.

Claim 6. (Original) The electronic system of claim 5 wherein the pull-up device has a gate coupled to a first predriver circuit, and the pull-down device has a gate coupled to a second predriver circuit.

Claim 7. (Original) The electronic system of claim 6 wherein the integrated circuit further comprises:

a core comprising a plurality of logic gates, and one of the logic gates is coupled to provide a signal to the first predriver.

Claim 8. (Original) The electronic system of claim 6 further comprising a switch coupled between the pad and clamp diode.

Claim 9. (Currently amended) An electronic system comprising:

a first integrated circuit comprising:

an input buffer coupled between a first supply terminal and a second supply terminal and having an input directly connected to a pad; and

a series of clamp diodes coupled between the pad and the second supply terminal; ~~and~~

a resistor having a first terminal coupled to the pad, and a second terminal coupled to receive an input signal; and

a second integrated circuit coupled to the second terminal of the resistor to provide the input signal,

wherein the resistor is not on the first integrated circuit or the second integrated circuit.

Claim 10. (Original) The electronic system of claim 9 wherein the series of clamp diodes comprises four diodes.

Claim 11. (Currently amended) The electronic system of claim 10 further comprising:

a pull-up output device coupled between the first supply terminal and the pad, wherein a well of the pull-up device is coupled to the first supply terminal ~~a second integrated circuit coupled to the second terminal of the resistor to provide the input signal~~.

Claim 12. (Previously presented) The electronic system of claim 9 wherein each of the clamp diodes in the series of clamp diodes has an anode and a cathode, the anode of one of the clamp diodes in the series of clamp diodes is coupled to the pad, and the cathode of one of the clamp diodes in the series of clamp diodes is coupled to the second supply terminal.

Claim 13. (Previously presented) The electronic system of claim 12 wherein the first supply terminal receives a positive supply voltage, and the second supply terminal receives a ground supply.

Claim 14. (Previously presented) The electronic system of claim 9 wherein the integrated circuit further comprises:

a pull-up output device coupled between the first supply terminal and the pad; and

a pull-down output device coupled between the pad and the second supply terminal.

Claim 15. (Original) The electronic system of claim 14 wherein the pull-up device has a gate coupled to a first predriver circuit, and the pull-down device has a gate coupled to a second predriver circuit.

Claim 16. (Original) The electronic system of claim 15 wherein the integrated circuit further comprises:

a core comprising a plurality of logic gates, and one of the logic gates is coupled to provide a signal to the first predriver.

Claim 17. (Previously presented) An integrated circuit comprising:

a buffer having a first supply terminal, a second supply terminal, and an input;

a clamp circuit coupled between the input of the buffer and the first supply terminal of the buffer; and

a resistor coupled to the input of the buffer,

wherein the clamp circuit comprises a clamp diode in series with a switch, the switch capable of closing if opened and opening if closed under control of a first signal.

Claim 18. (Original) The integrated circuit of claim 17 wherein the resistor is further coupled to a pad.

Claim 19. (Original) The integrated circuit of claim 18 wherein the clamp circuit comprises one diode having an anode and a cathode, the anode coupled to the input of the buffer and the cathode coupled the first supply terminal.

Claim 20. (Original) The integrated circuit of claim 19 wherein the clamp circuit comprises a series of diodes each having an anode and a cathode, the anode of a first diode in the series of diodes coupled to the input of the buffer, and the cathode of a last diode in the series of diodes coupled to the first supply terminal.

Claim 21. (Original) The integrated circuit of claim 18 further comprising:

an output driver comprising:

a pull-up device coupled between the first supply terminal and the input of the buffer; and

a pull-down device coupled between the input of the buffer and the second supply terminal.

Claim 22. (Previously presented) The integrated circuit of claim 17 wherein the switch is a transistor having a gate coupled to receive the first signal.

Claim 23. (Previously presented) The electronic system of claim 1 wherein the integrated circuit further comprises a transistor in series with the clamp diode, the transistor having a gate coupled to receive a control signal.

Claim 24. (Previously presented) The electronic system of claim 23 wherein the control signal is provided by a memory cell.

Claim 25. (Previously presented) The electronic system of claim 1 wherein the integrated circuit further comprises:

a first transistor in series with the clamp diode, the transistor having a gate coupled to receive a control signal; and

a second transistor coupled between the pad and the first supply terminal,

wherein the clamp diode is a drain-to-bulk diode of the second transistor.

Claim 26. (Previously presented) The electronic system of claim 1 wherein the integrated circuit further comprises:

a pull-up transistor coupled between the pad and the first supply terminal;

a first transistor coupled between the pad and a bulk of the pull-up transistor; and

a second transistor coupled between the bulk of the pull-up transistor and the first supply,

wherein the clamp diode is a drain-to-bulk diode of the pull-up transistor.

Claim 27. (Currently amended) An electronic system comprising:

an integrated circuit comprising:

an output buffer comprising a pull-up transistor coupled between a pad and a first supply voltage;

a first transistor coupled between a bulk of the pull-up transistor and a source of the pull-up transistor, and having a gate coupled to receive a control signal; and

a second transistor coupled between a drain of the pull-up transistor and the bulk of the pull-up transistor, and having a gate coupled to receive a complement of the control signal;

a hot-socket circuit coupled to the pad and the first supply voltage, wherein the hot-socket circuit provides an output having a first state if a voltage on the pad is higher than the first supply voltage and a second state if the voltage on the pad is lower than the first supply voltage; and

a logic circuit coupled to receive the output of the hot-socket circuit and an enable signal and to provide the control signal,

wherein when the control signal is in a first state, the bulk of the pull-up transistor is coupled to the pad, and when the control signal is in a second state, the bulk of the pull-up transistor is coupled to the first supply voltage, and a drain-to-bulk diode of the pull-up transistor clamps a voltage received at the pad, and when the enable signal is in a disable state, the bulk of the pull-up device is coupled to the first supply voltage.

Claim 28. (Previously presented) The electronic system of claim 27 further comprising:

a resistor coupled to the pad and further coupled to receive an input signal.

Claim 29. (Previously presented) The electronic system of claim 28 wherein the integrated circuit further comprises:

an input buffer coupled between the first supply voltage and a second supply voltage and having an input directly connected to the pad.

Claim 30. (Currently amended) The electronic system of claim 28 wherein the logic circuit is an AND gate ~~integrated circuit further comprises:~~

~~a hot-socket circuit to provide the control signal, wherein the hot-socket circuit determines the higher voltage between the voltage on the pad and the first supply voltage~~.

Claim 31. (Previously presented) The electronic system of claim 28 wherein the integrated circuit further comprises:

a plurality of programmable logic elements configurable to implement user-defined logic functions.

Claim 32. (New) An electronic system comprising:

a first integrated circuit comprising:

a pull-up transistor coupled between a first supply voltage and a pad;

a pull-down transistor coupled between the pad and a second supply voltage;

a clamp circuit comprising a diode and a first transistor coupled as a switch, the clamp circuit coupled between the pad and the first supply voltage;

a well-bias circuit coupled to provide the higher voltage between a voltage on the pad and the first supply voltage to a well of the pull-up transistor and the first transistor.

Claim 33. (New) The electronic system of claim 32 further comprising:

a resistor having a first terminal coupled to the pad, and a second terminal coupled to receive an input signal; and

a second integrated circuit coupled to the second terminal of the resistor to provide the input signal,

wherein the resistor is not on the first integrated circuit or the second integrated circuit.

Claim 34. (New) The electronic system of claim 32 wherein the integrated circuit further comprises:

an input buffer coupled between the first supply voltage and a second supply voltage and having an input directly connected to the pad.

Claim 35 (New) The electronic circuit of claim 32 wherein the pull-up transistor has a gate coupled to a first predriver circuit, and the pull-down transistor has a gate coupled to a second predriver circuit.